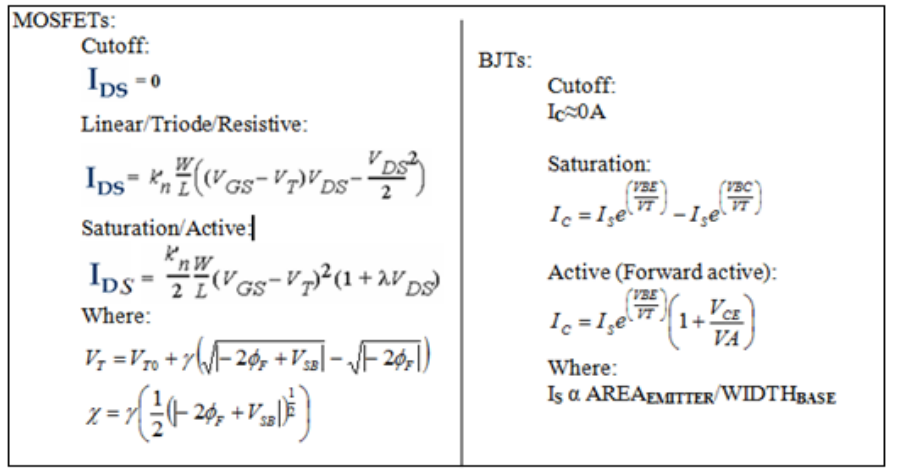
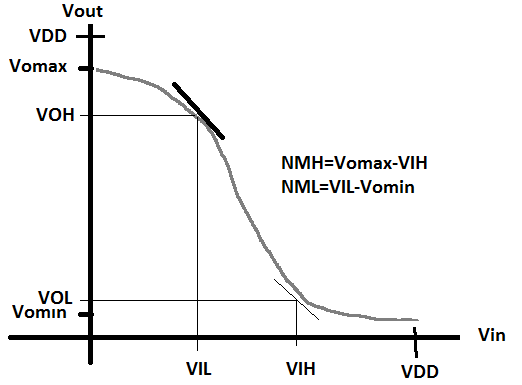
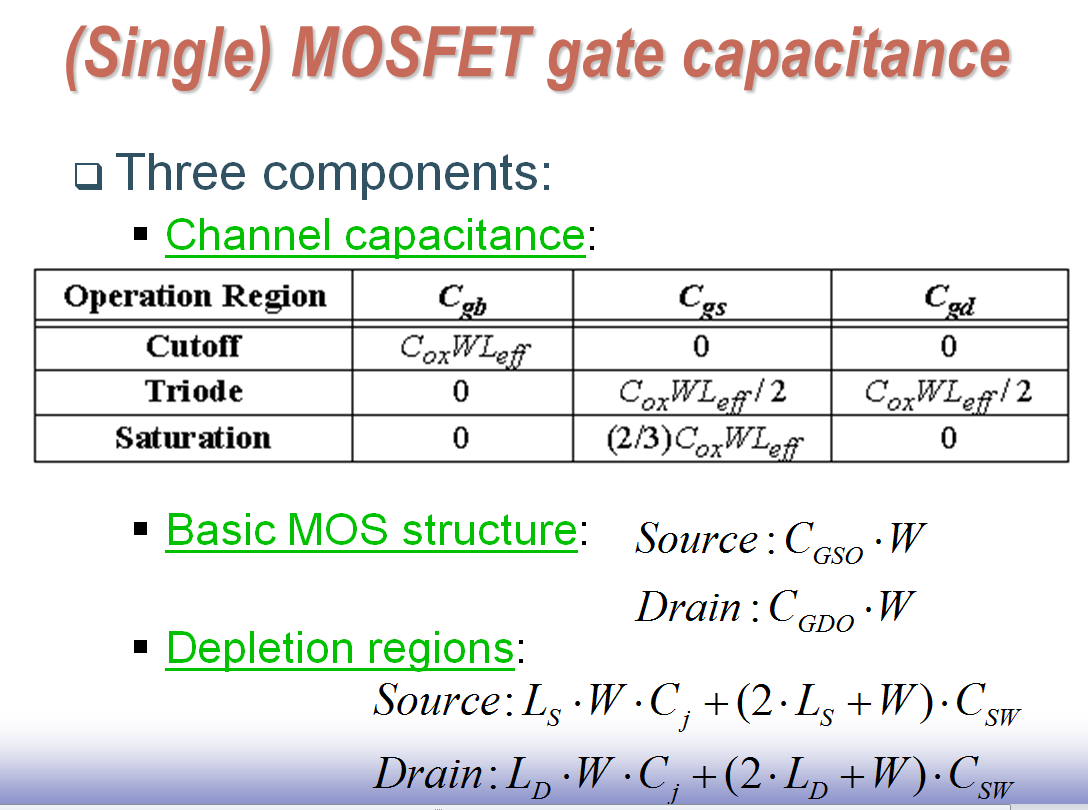
**EE307 Digital Electronics and Integrated Circuits**

**Class Midterm**, **February 24, 2017**

Delay: 

Power: 





**=CGC**

Definition: VTC or transfer characteristics: Vout on Y-axis, Vin on X-axis. More generally: Input on X-axis, output on Y-axis.

Definition of “Forward active” for BJTs includes both VCEsat and PN junction requirements.

**>> COMMENT DURING EXAM:**

Saturation=Active=pinchoff

Triode=resistive=Ohmic=linear

Cutoff=cutoff

No calculators.

Only the attached cheat sheet allowed.

No cheating.

Show work where asked (or no credit!).

Rules:

**NAME:** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

I promise not to discuss this exam with those that have not taken it yet.

Signature:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_



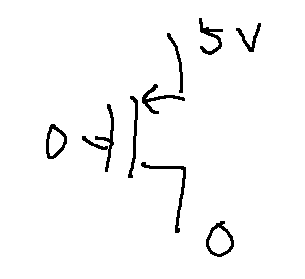
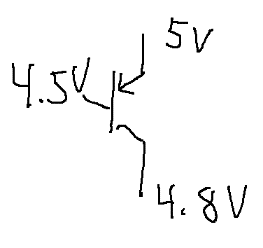
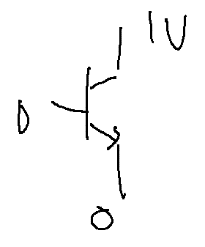
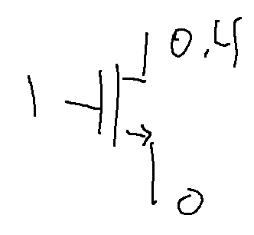
|  |  |  |
| --- | --- | --- |
| Question | Pts | Score |
| Did you write your name? | 5 |  |
| 1a-c | 24 |  |
| 2a-g | 35 |  |
| 3 | 12 |  |
| 4 | 8 |  |
| 5a-d | 16 |  |
| Total | 100 |  |

**EXAM:**

1. Regions of operation. VBEon**NPN**=0.5V, VBEon**PNP**=-0.6V, VCEsat**NPN**=0.2V, VCEsat**PNP**=-0.3V, VT**NMOS**=0.5V, VT**PMOS**=-0.5V, VA=100, λ**N**=0.03V**-1**, and λ**P**=0.03V**-1**.
   1. Draw the transistors and voltages at the terminals to put the following transistors into the specified region of operation. Put a voltage value on the terminal – Don’t put the difference in terminals. In other words, specify VG, not VGS. **(Total: 12pts=4x3pts)**
      1. PMOS in active
      2. pnp in linear
      3. npn in cutoff
      4. NMOS in linear

**ANSWER:**

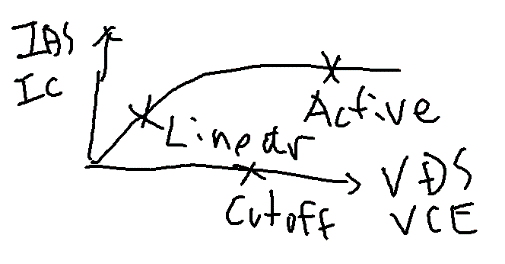
i Active ii linear iii cutoff iv linear

**-1 symbol**

* 1. Draw the IDS vs VDS graph for an NMOS and mark three points. One that can only be in active, one point that can only be in linear and one that can only be in cutoff. **(Total: 4pts)**

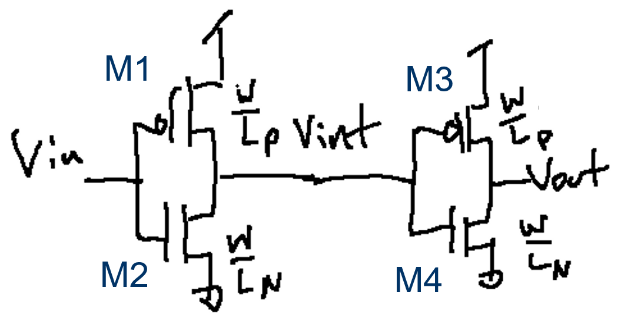
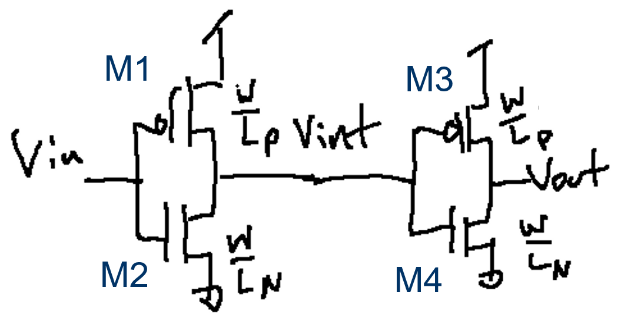
**ANSWER:**



* 1. In Circuit 1, Vin=0 for long enough that Vint and Vout are not moving anymore and are sitting at DC voltages. Then Vin changes instantaneously from 0 to VDD. **(Total: 8pts=4x2pts)**
     1. What region of operation is M1 in **right** after the Vin transition from 0 to VDD in Circuit 1?
     2. What region of operation is M2 in **right** after the Vin transition from 0 to VDD in Circuit 1?
     3. What region of operation is M3 in **right** after the Vin transition from 0 to VDD in Circuit 1?
     4. What region of operation is M4 in **right** after the Vin transition from 0 to VDD in Circuit 1?

**ANSWERS:**

i Cutoff, ii Active iii Cutoff iv Linear



**0🡪VDD**

**0**

**VDD**

Circuit 1

**-1 if cutoff at origin**

1. Capacitances and resistances. We will use the rules that we used in class for Circuit 1: **(Total: 35pts=7x5pts)**

**RULES for all questions about circuit 1**

* + **Vin moves instantaneously**
  + **Vint takes some time to change but it does change**
  + **Vout: Assume Vout doesn’t move while Vint is changing**
  1. In Circuit 1, Vin=0 for long enough that Vint and Vout are not moving anymore and are sitting at DC voltages. What is the capacitance on Vin for a transition from Vin=0 to Vin=VDD? Answer using CGSov etc. **(The complete description of C seen at this node from the transistors)**

**ANSWER: With Miller for full points.**



* 1. Replace each term of the equation you found in question 2a with the detailed equations that you’d use to find an actual numerical value for the capacitance.

**ANSWER:**



* 1. In Circuit 1, Vin=0 for long enough that Vint and Vout are not moving anymore and are sitting at DC voltages. What is the capacitance on Vint for a transition from Vin=0 to Vin=VDD? Answer using CGSov etc.

**ANSWER:**



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | IDS (mA) | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  | -4.5 | | -4.0 | | -3.5 | | -3.0 | | -2.5 | | -2.0 | | -1.5 | | -1.0 | | -0.5 | |  |  | 0.5 | | 1.0 | | 1.5 | | 2.0 | | 2.5 | | 3.0 | | 3.5 | | 4.0 | | VDS |
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* 1. For VDD=4V, set up the equation to find Ron**NMOS** using the single point approximation.

**ANSWER:**



* 1. For VDD=4V, set up the equation to find Ron**PMOS** using the two point approximation.

**ANSWER:**



* 1. Calling the answer to question 2a, C**Q2a**, the answer to question 2c, C**Q2c**, Ron**NMOS** (from question 2d) and Ron**PMOS** (from question 2e), what is the equation for the propagation delay at Vint? **(Transition of Vin=0 to Vin=VDD)**

**ANSWER:**



* 1. What is the difference between the propagation delay and rise/fall times? I’m not talking about the equation – I’m talking about how what they measure is different.

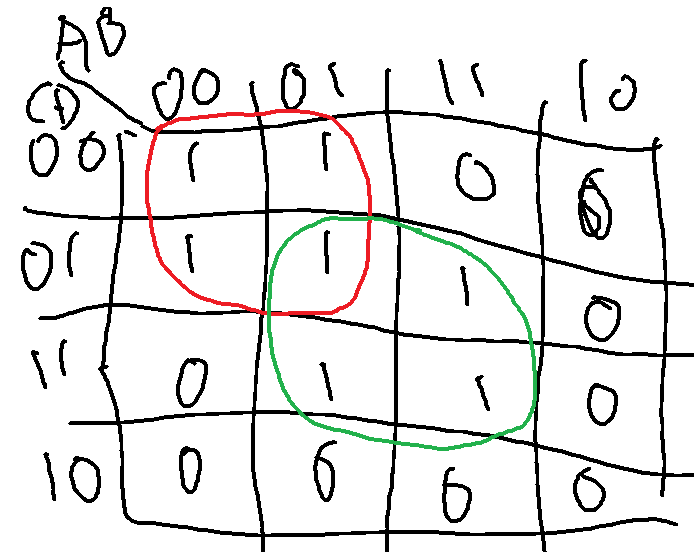
**ANSWER:**

Propagation delay is through a circuit. You change the input to the circuit and see how long until the output changes. 50% of the input to 50% of the output. Rise time and fall time is watching a single wire at one point and seeing how long it takes the wire to go from 10% to 90% of transition.

1. For the following truth table, use a Kmap to create (the simplest) logic and then create a complex CMOS circuit. Show all work for full credit. **(12pts)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input | | | | Output |
| A B C D | | | |  |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**ANSWER:**





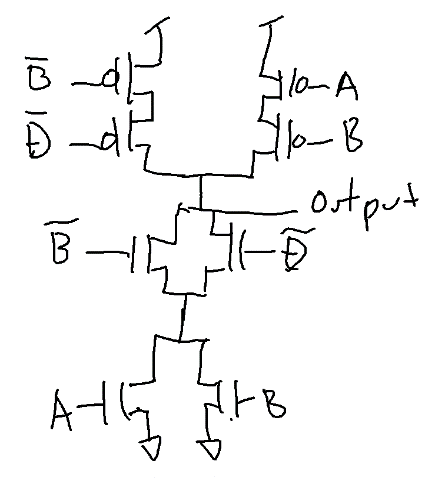
To find PDN:



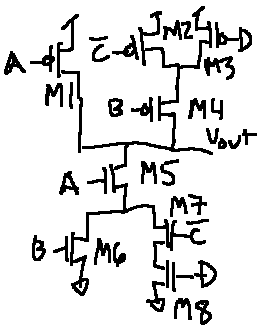
Inputs are:



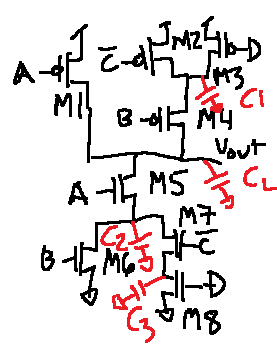
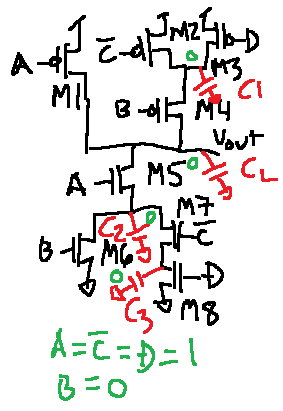
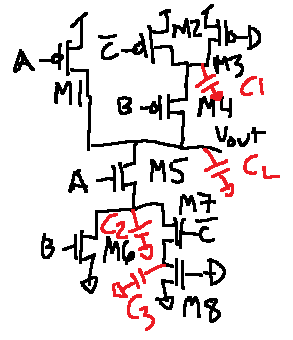
CMOS circuit is:



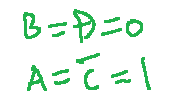
1. Find τ using the Elmore delay technique for the worst case low to high transition for Circuit 2. Show important diagrams so I can see where equation(s) come from. Use subscripts on all Rs and Cs so I can tell where each comes from. **(Show all work. Name all Rs & Cs).** **(8pts)**

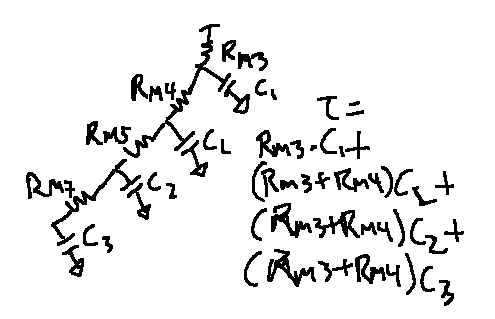


**ANSWER:**



Then:





1. Short questions: **(Total 16pts=4x4pts)**
   1. What are the three types of power that a CMOS circuit uses? Describe each type of power.

**ANSWER:**

Dynamic: Current used to charge up capacitance on output.

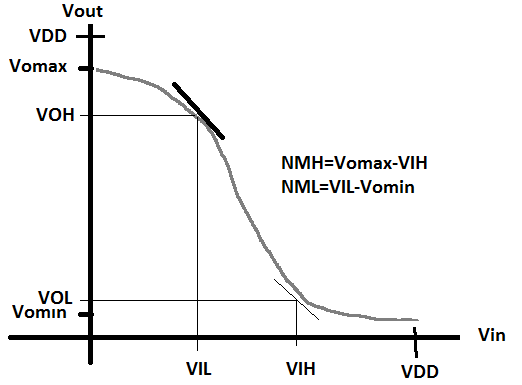
Short-circuit: During transition, when both transistors are on, current goes straight from supply to GND.

Leakage current: When holding a value, the transistors in cutoff leak and the amount leaked is recharged from the supply.

* 1. Explain noise margins.

**ANSWER:**

Noise margins are when two circuits are cascaded. The output of the first circuit is the input to the second circuit. The total range of the output of the first circuit is the total range of the input to the second circuit. The second circuit has part of its input range that’s in an undefined region. On either side of the undefined region the second circuit works well and outputs a solid ‘1’ or ‘0’. The width of the region that is inside the input range and is a solid ‘1’ is one noise margin and the input range and is a solid ‘0’ is another noise margin. The width of each noise margin is how much noise you can have on the input for each output value. Not a great explanation…..



* 1. What is happening when the voltage on a node changes?

**ANSWER:**

The capacitance on the node is getting charged up.

* 1. Is a VTC found using a DC sweep simulation or a transient response simulation? Why?

**ANSWER:**

DC sweep. The VTC is a DC graph and transient response is a time dependent graph.